Welcome to the « SPEAr Age »
Structured Processor Enhanced Architecture

SPEAr:
an HW/SW reconfigurable
multi processor architecture
Outline

- Economics of Moore’s law and market view
- Spear™ architecture
- From single core to dual core
- Development flow
- Application examples
- Conclusions
Moore’s laws:
- every 18 months chip complexity doubles
- cost of fabs will double from one generation to the next

![Graph showing the growth of transistors/chip and costs from 1970 to 2010.](image)
The reality

- Die size almost constant with new technologies
  - more functions integrated

- NREs more than double from one generation to the next
  - Cost of masks double from one generation to the next
  - Development costs increase exponentially

- Revenues for each ASIC is not growing like investments

- 61% of designs requires at least one respin
Once upon a time there was the Single Function printer, only capable to print a document from a PC.

It then became a 3-1 Multifunction, capable of printing, scanning and faxing documents.

It further evolved into a 4-1 Multifunction, capable of printing high quality pictures, working as a stand alone photocopier and with networking capabilities.

It finally became an “Easy-to-use” stand alone printing tool for your pictures.

... and small businesses are proliferating.
The economics are changing ...

<table>
<thead>
<tr>
<th>ASIC Model</th>
<th>Few new models per / year</th>
<th>Many new models per / year</th>
</tr>
</thead>
<tbody>
<tr>
<td>HW cost is predominant</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW cost is predominant</td>
<td></td>
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</tbody>
</table>

... but proprietary technologies continue to be a differentiation factor

Is the Full Asic a sustainable model ?
What the market is looking for

- A good, standard and powerful architecture based on standard IPs
  - easy to reuse
  - easy to migrate to different technology and different silicon vendors

- Easy access to leading edge technologies
  - lower power consumption
  - higher speeds
  - more functions

- Fast turn around time
  - market is volatile, pervasion of new technologies is very rapid

- Simple and early system development
  - the ASIC or the IC is just a small part of the system
  - SW is playing a key role
SPEAr concept

Pre-Fabricated set of logic functions

Customized selected few routing tracks

With change of few mask layers, additional Customer IPs can be added to the base “SPEAr” device

PreFabricated Top Layers

Metal Info

Via Info

Metal Info

PreFabricated Base Layers
SPEAr™: The architecture
Setting the stage
SPEArHead200: single processor

- Introducing SPEArHead200 - the first Configurable SOC
- Based on a robust state of the art architecture, IP selection and core (ARM9 266Mhz supporting MMU)
- Including 200 Kgates of configurable logic
- Introducing a new development methodology
- Dramatically reducing cycle times
  - 6 weeks vs. 6 months for silicon re-spins
- Dramatically reducing NRE
  - Typically 1/5 of a full asic NRE
- First Silicon since Q4/2005
State of the Art Architecture & IPs

32 bit AHB Bus

- Vectorized Interrupt
- MII 10/100
- DMA MII
- USB PHY
- UDC 2.0
- UDC AHB
- USB PHY
- UHOSTC 2.0
- UHOSTC AHB
- USB PHY
- UHOSTC 2.0
- UHOSTC AHB

32 bit APB Bus

- ARM926EJS
- -1 cache 32K
- -Dcache 16K
- -ETM9
- -Coproc.
- Timer
- GPIO
- Uart
- APB
- Int ctr
- Misc Reg
- UART
- RTC
- GPT
- GPIOs
- WDT
- I2C
- PLL2 cfg
- PLL1 cfg
- ADC

AHB Bus Matrix

MPMC

SDRAM/DDR

Serial Flash

APB bridge

EBI
Support for System Development

- 32 bit AHB Bus
  - Vectorized Interrupt
  - MII 10/100
  - DMA MII

- 32 bit APB Bus
  - Master
  - Slave #1
  - Slave #2

Programmable Logic
- 200K gates
- ARM926EJ-S
  - -L cache 32K
  - -Dcache 16K
  - -ETM9
  - -Coproc.
- Timer
- GPIO
- UART
- APB
- Int ctr

AHB SubSystem
- SDRAM/DDR
- MPU
- MPMC
- EBI
- USB Plug Detect
- USB Phy

Miscellaneous
- Misc Reg
- UART
- RTC
- GPT
- GPIOs
- WDT
- I2C
- PLL2 cfg
- PLL1 cfg
- ADC

Support for System Development

- Development
Innovative System Development

Configuration pad set to “development mode”

FPGA Top Level (ST)

FPGA

Customer Logic

Port Ctrl

I/O

GP I/O

RTL Design (Customer)

Once the application is working the RTL is extracted from the FPGA and it is converted into config. logics
SPEAr Development Board

- FPGA: Xilinx XC3S4000
- Flash: For FPGA
- Serial Flashes: Up to 32 MB
- Ethernet PHY
- 32 Mbyte DDR

It comes equipped with a suite of drivers for all the peripherals, supporting Linux and WxWorks Operating Systems, supporting simple JTAG based emulators.
Supporting Multiple Interfaces

- Expansion Lines (120 I/Os)
- 3 Serial I/F
- 2 USB 2.0 Host Ports HS Capable
- 1 USB 2.0 Device
- 16 ADC Channels
- 6 GPI/O Lines
- FPGA JTAG I/F
- Ethernet 10/100
- ETM9 I/F 24 bit
- JTAG I/F

Make ASIC easy
FW/SW Partitioning

- ARM core, equipped with Linux (core 2.6.10 Montavista) or VxWorks
  (extension to Windows CE in evaluation)
  - OS
  - Connectivity
  - Application layers
  - Real time operations

- Customizable logic for hardware accelerators & specific IPs
Moving to dual processor: SPEArPlus600

- Addressing market segmentation
- Higher Computation Power with lower power consumption
- Second Arm to boost performance
  - Easier to use than a dedicated DSP
  - Backward compatible
- SPEArPlus silicon in Q1/2007
- Full reference platform for Printers
- Expanding into side applications (NAS)
Main highlights:
- 600 Kgates progr logic array
- 2 ARM926EJS @333MHz
- Dithered PLL
- 1 USB2.0 device
- 2 USB2.0 host
- DDR1+DDR2 COMBO PHY
- CMOS SRC 3.3V, LVDS 2.5V
- 2 Oscillators
- ADC 8 channels, 10bits

Package: PBGA 420 23x23
Technical Characteristics

- Dual 333Mhz ARM926 16k+16k Architecture
  - Potential TCM extension (up to 32k+32k)
  - 720 (2 x 360) Mips Drystone 2.1
- 600k gate of configurable logic
- From 1 to 4 Metals needed to be specialized
- Ethernet GMAC + USB2.0 Triphy, Timers, RTC, 2 UARTs, 3SPI, IRDA, I²C
  - USB: 1 Device port + 2 Host ports
- Jpeg accelerator, Display controller XGA 1024x768, color TFT panel
- 4 High Performance Memory controller
  - SDRAM, DDR1/2, Serial Flash, Nand Flash
  - 32bit bus @ 166MHz, total 664 MBytes/Sec
- 136 KB SRAM & 32KB ROM
- High Performance System Architecture
  - High speed I/Os overall throughput: ~ 305MByte/sec
  - Four channel DMA 32bit @ 166Mhz: ~ 664MByte/sec
- Package PBGA 420 balls, 23x23mm, 1 mm pitch
128KB+8KB Internal SRAM memory

- **32KB**
  - 8 blocks: 8KB
  - 4 blocks: 2KB

- **96KB Single Port**
  - 8 blocks: 4KB

- **32KB**
  - 16 blocks: 32KB

- **32KB Dual Port**
  - 8 blocks: 2KB
  - 4 blocks: 4KB

Dual Port memory can be increased using Single Memory Port in arbitrate mode.

**Maximum flexibility in grouping memory blocks**
- e.g. 10KB = 1 block 8KB + 1 block 2KB...
Multi – Core FW/SW Partitioning

- ARM 1, equipped with Linux (core 2.6.10 Montavista), is used to run:
  - Job Manager & Connectivity
- ARM2, equipped with RTOS, is used to run:
  - Image pipeline & Real time operations

- Customizable logic for hardware accelerators
Application examples: MPEG4 decoding
Case study: MPEG4 decoder

Full SW solution

- Maximum performances on one ARM926
  - 18fps if ARM running at 266MHz
  - 22fps if ARM running at 333Mhz

- CPU load for a MPEG4 stream simple profile, lev.0-3

![Performance Requirements Table]

<table>
<thead>
<tr>
<th></th>
<th>QCIF</th>
<th>QVGA</th>
<th>CIF</th>
<th>VGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Rate</td>
<td>15fps</td>
<td>15fps</td>
<td>30fps</td>
<td>30fps</td>
</tr>
<tr>
<td>Bit Rate</td>
<td>64kbps</td>
<td>256kbps</td>
<td>384kbps</td>
<td>1Mbps</td>
</tr>
<tr>
<td>External Memory (excl. post processing)</td>
<td>80kB</td>
<td>238kB</td>
<td>313kB</td>
<td>930kB</td>
</tr>
<tr>
<td>CPU Load</td>
<td>16MHz</td>
<td>50MHz</td>
<td>130MHz</td>
<td>400MHz</td>
</tr>
<tr>
<td>Memory Footprint (inc. program code, ROM data and RAM data)</td>
<td>51kB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
MPEG4 decoder

**HW/SW solution**

- **HW accelerator implemented in programmable logic**
  - to accelerate the more complex functions of the SW decoder
  - size of the accelerator is 150k gates + 15kB SRAM running at 66MHz
  - load of CPU is <10MHz
  - VGA resolution 30 fps at 333MHz
Possible SoC resources usage

<table>
<thead>
<tr>
<th>ARM1</th>
<th>ARM2</th>
<th>User logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free for any usage</td>
<td>100%</td>
<td>Non additional logic needed</td>
</tr>
</tbody>
</table>

Full SW solution (ARM running at 266Mhz)

<table>
<thead>
<tr>
<th>ARM1</th>
<th>ARM2</th>
<th>User logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free for any usage</td>
<td>5%</td>
<td>150 kgate</td>
</tr>
</tbody>
</table>

HW/SW solution
Application examples: FAX function
## FAX Soft Modem Linux Driver – Class 1

### FAX Software – Modem Class 1

<table>
<thead>
<tr>
<th>FAX APPLICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Image conversion, compression - ITU-T T.4/T.6</td>
</tr>
<tr>
<td>• MH, MR (G3), MMR (G4), JBIG (ITU-T T.82), JPEG (ITU-T T.81)</td>
</tr>
<tr>
<td>• User interface</td>
</tr>
<tr>
<td>• Scanning and printing</td>
</tr>
</tbody>
</table>

### Manage FAX session (ITU-T.30)

- Exchange and agrees with remote FAX the printing capabilities
- Exchange and agrees with remote FAX the session and transmission capabilities (protocol, speed, ECM, ...)
- Send / Receive data file in blocks / packets
- Implement retransmission of bad packets (ECM option)

### Interface between Application and Driver with AT CMD (Class 1) – ITU-T T.31

<table>
<thead>
<tr>
<th>FAX (Soft) Modem DRIVER - (Class 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Linux serial driver interface</td>
</tr>
<tr>
<td>• AT CMD interpreter (ITU-T T.31)</td>
</tr>
<tr>
<td>• Modem state machine</td>
</tr>
<tr>
<td>• Connection protocol (ITU-T V.21) with remote FAX</td>
</tr>
<tr>
<td>• Data Modulation (DATA PUMP) – V27ter, V.29, V.17, V.34 H/D</td>
</tr>
<tr>
<td>• Interface with HW driver (STLC7550)</td>
</tr>
</tbody>
</table>

Both running on ARM926
Possible SoC resources usage

(ARM running at 266Mhz)

ARM1: Free for any usage

ARM2: 15% FAX, 5% MPEG4 30fps, 20kg user logic

150 kgate
Conclusions

- SpearPlus architecture opens the door to unprecedented flexibility
  - HW configurability
  - dual core SW configurability
- Symmetrical dual core architecture for maximum flexibility
  - Possibility to map different OS
  - Possibility to access all the peripherals from the 2 cores
  - Possibility to access programmable logic from the 2 cores
- HW flexibility
  - configurable logic on board
  - possibility to use embedded SRAm as TCM of ARM cores
Moving to dual processor

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