Welcome to the « SPEAr Age »

Structured Processor Enhanced Architecture

SPEAr:

an HW/SW reconfigurable multi processor architecture

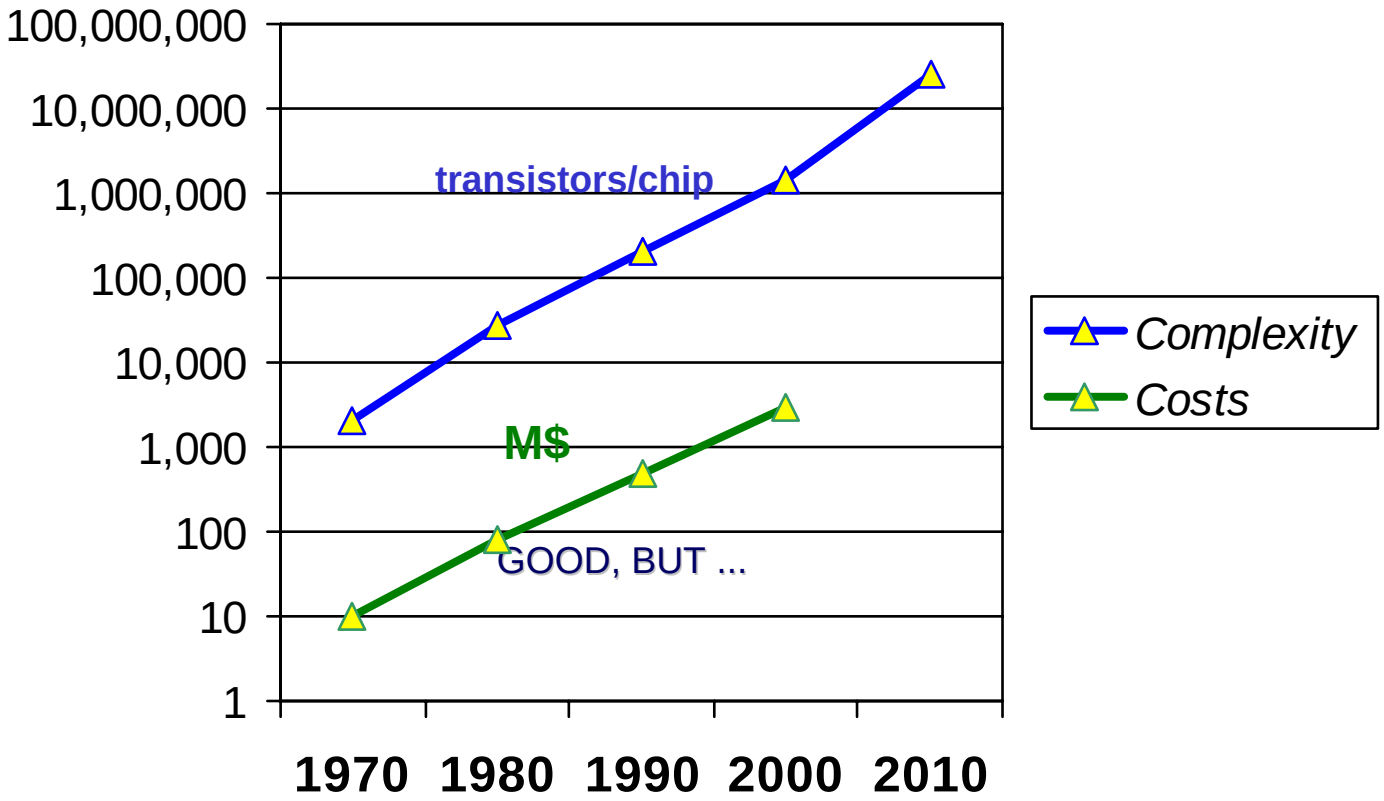
COMPUTER PERIPHERAL GROUP

Outline

- Economics of Moore's law and market view
- Spear™ architecture
- From single core to dual core
- Development flow
- Application examples
- Conclusions

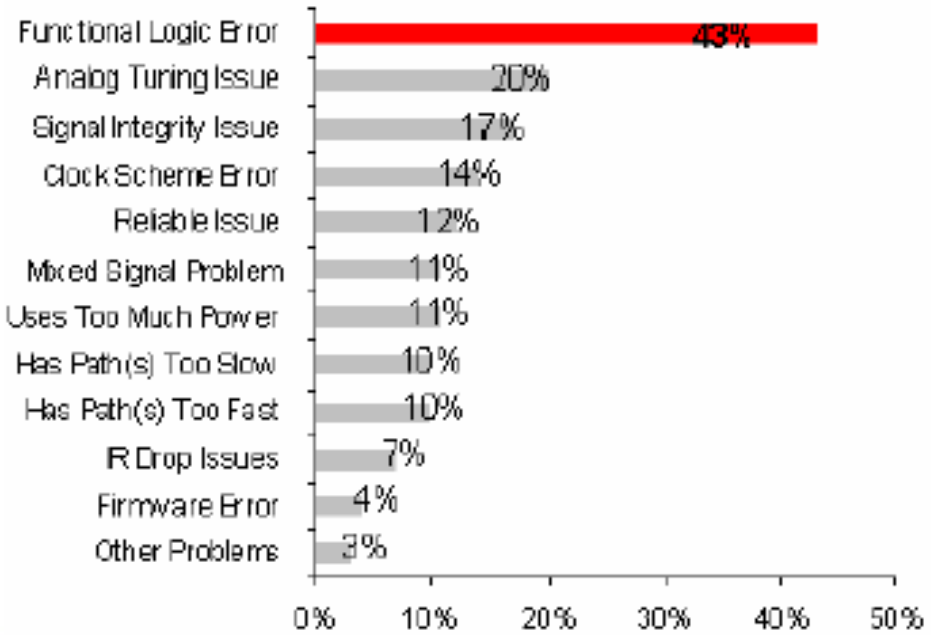
Moore's laws

- **Moore's laws:**
  - **every 18 months chip complexity doubles**
  - **cost of fabs will double from one generation to the next**



The reality

- Die size almost constant with new technologies
  - more functions integrated
- NREs more than double from one generation to the next
  - Cost of masks double from one generation to the next
  - Development costs increase exponentially
- Revenues for each ASIC is not growing like investments
- 61% of designs requires at least one respin



The Complexity is increasing …

- Once upon a time there was the Single Function printer, only capable to print a document from a PC

- It then became a 3-1 Multifuction, capable of printing, scanning and faxing documents

- It further evolved into a 4-1 Multifuction, capable of printing high quality pictures, working as a stand alone photocopier and with networking capabilities

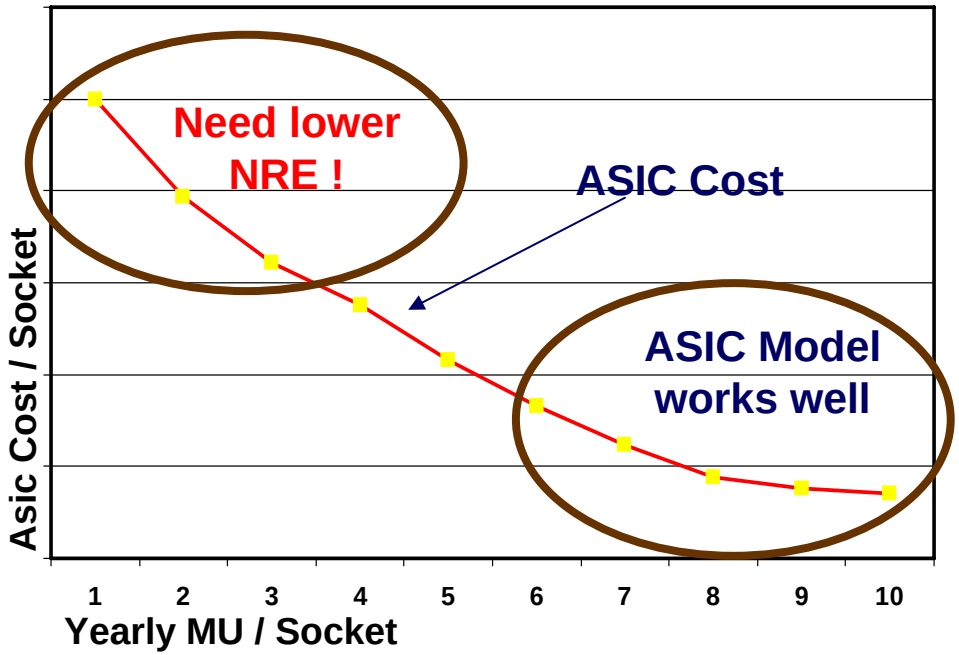
- It finally became an “Easy-to-use” stand alone printing tool for your pictures

… and small businesses are proliferating

The economics are changing …

Make ASIC easy

	Few new models per / year	Many new models per / year
HW cost is predominant	Market Trend	
SW cost is predominant		



… but proprietary technologies continue to be a differentiation factor

Is the Full Asic a sustainable model ?

What the market is looking for

- A good, standard and powerful architecture based on standard IPs
  - easy to reuse
  - easy to migrate to different technology and different silicon vendors
- Easy access to leading edge technologies
  - lower power consumption
  - higher speeds
  - more functions
- Fast turn around time
  - market is volatile, pervasion of new technologies is very rapid
- Simple and early system development
  - the ASIC or the IC is just a small part of the system
  - SW is playing a key role

SPEAr concept

Make ASIC easy

PreFabricated Top Layers

Metal Info

Via Info

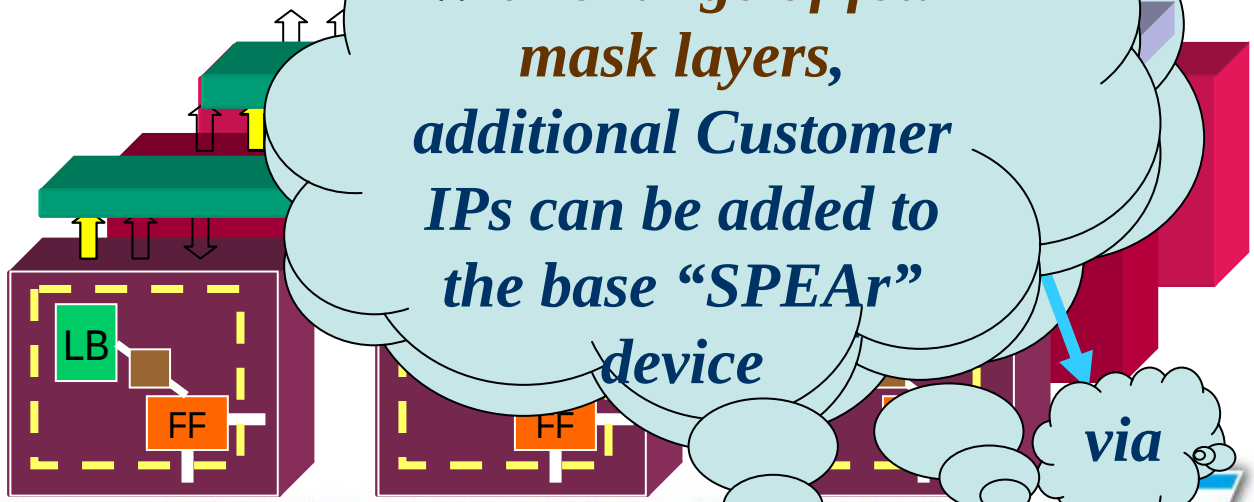
Metal Info

PreFrabricated Base Layers

Configurable SoC

Pre-Fabricated set of logic functions

Customized selected few routing tracks



With change of few mask layers, additional Customer IPs can be added to the base "SPEAr" device

via

SPEAr™:
The architecture

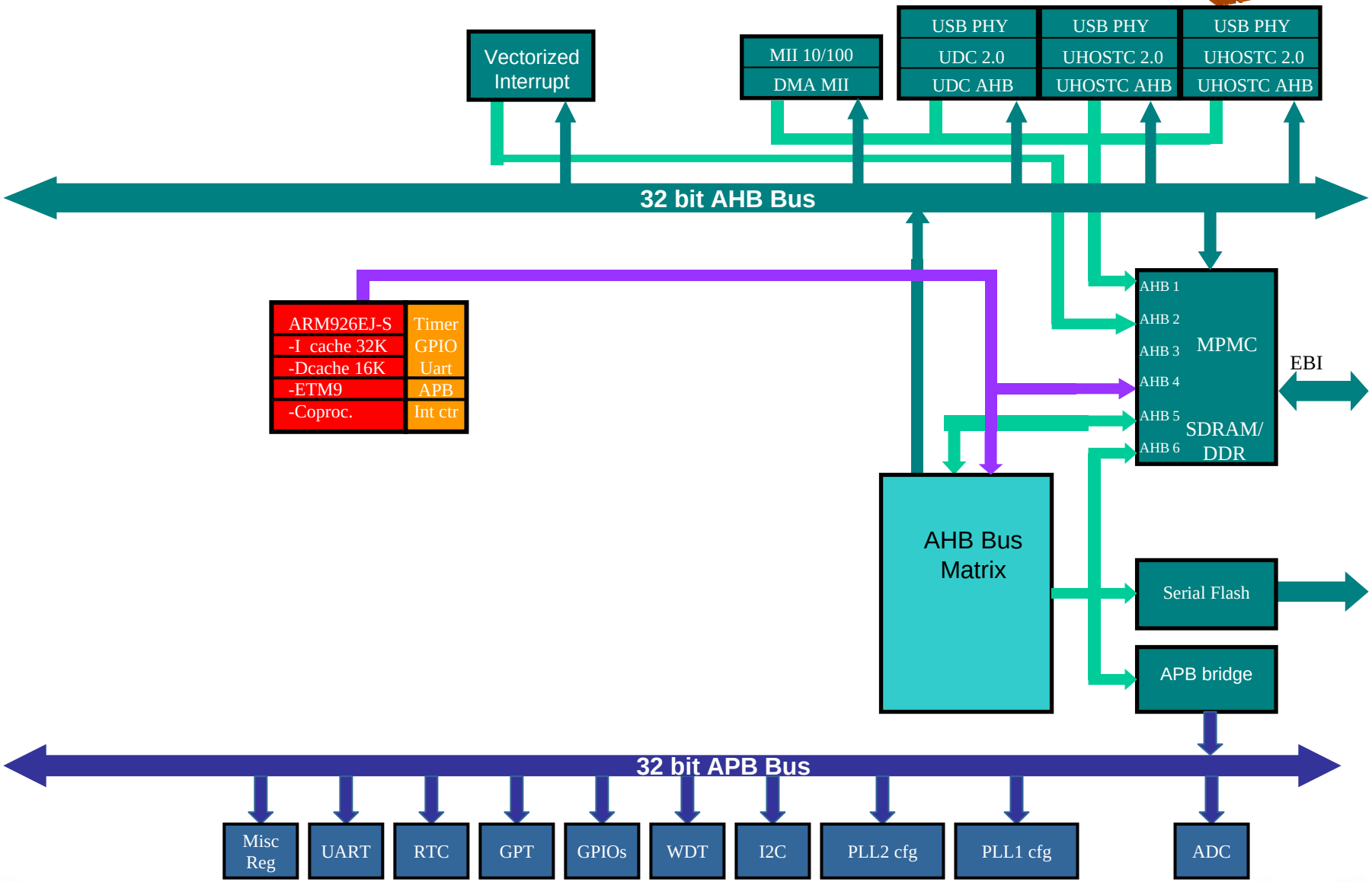
Setting the stage
SPEArHead200: single processor

- Introducing SPEArHead200 - the first Configurable SOC
- Based on a robust state of the art architecture, IP selection and core (ARM9 266Mhz supporting MMU)
- Including 200 Kgates of configurable logic
- Introducing a new development methodology
- Dramatically reducing cycle times
  - 6 weeks vs. 6 months for silicon re-spins
- Dramatically reducing NRE
  - Typically 1/5 of a full asic NRE
- First Silicon since Q4/2005

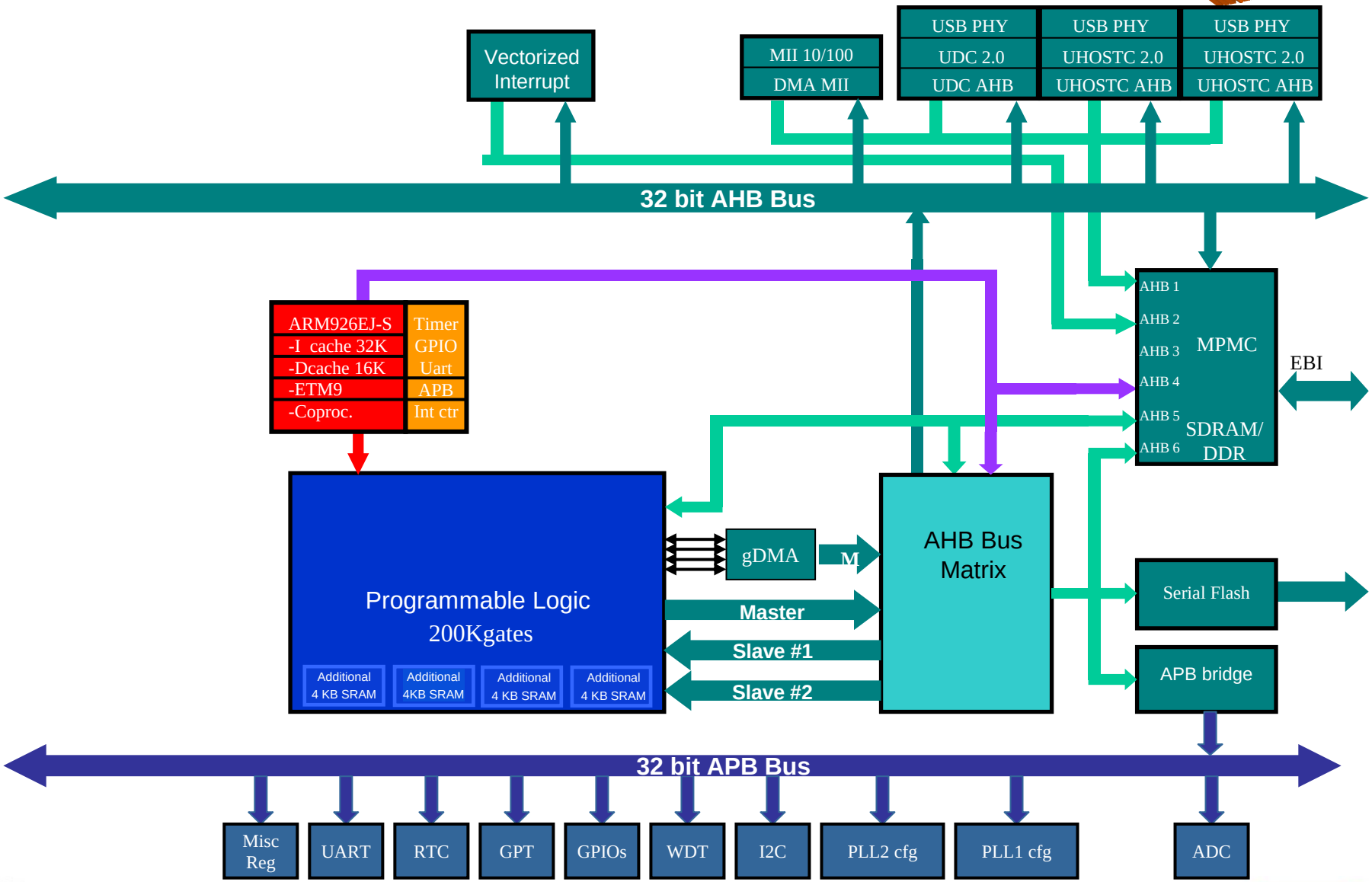
Configurable SOC
Single Core - 110nm

SPEArHead200
200kgate
ARM926@266MHz
BGA420

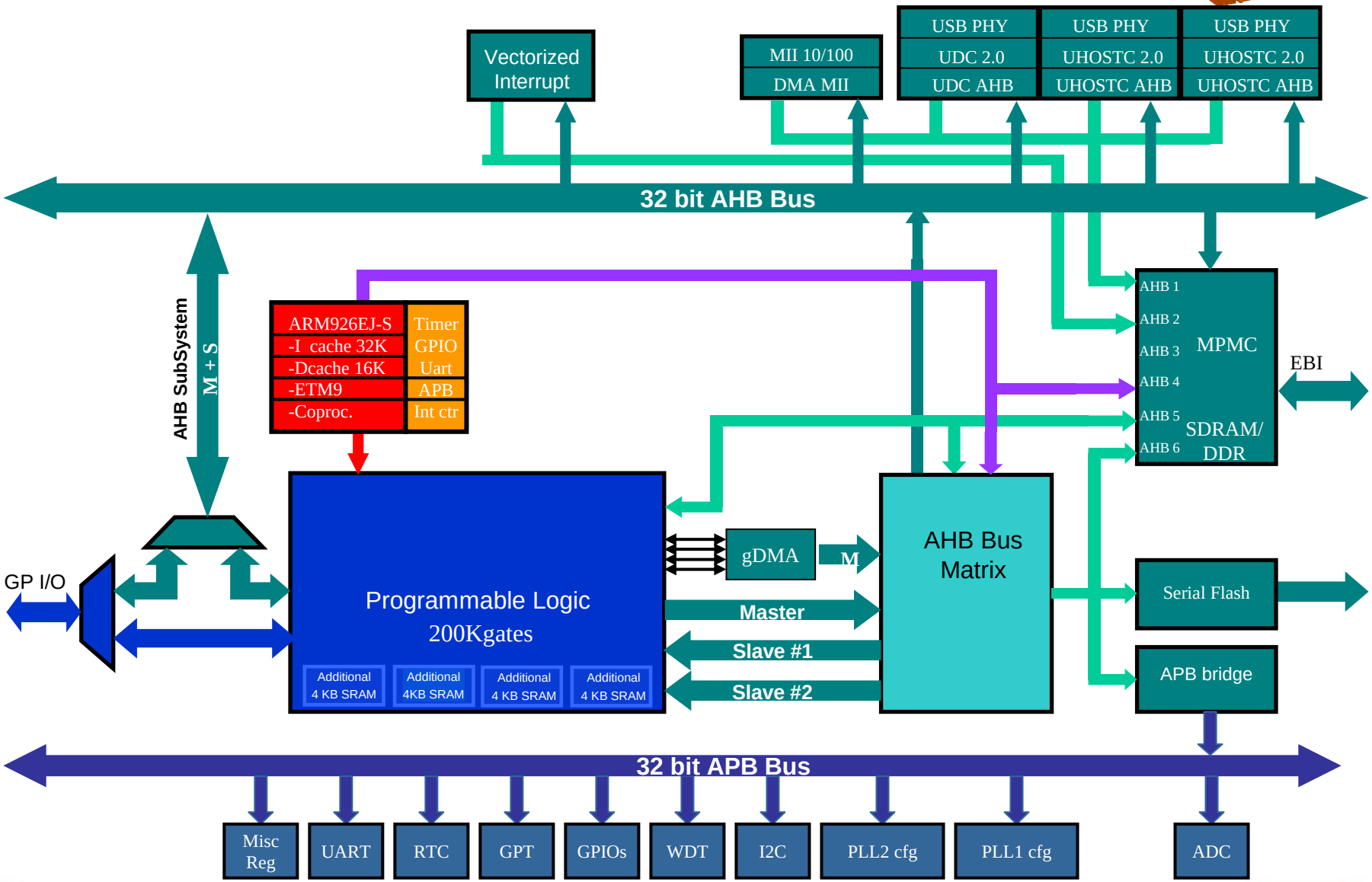
State of the Art Architecture & IPs



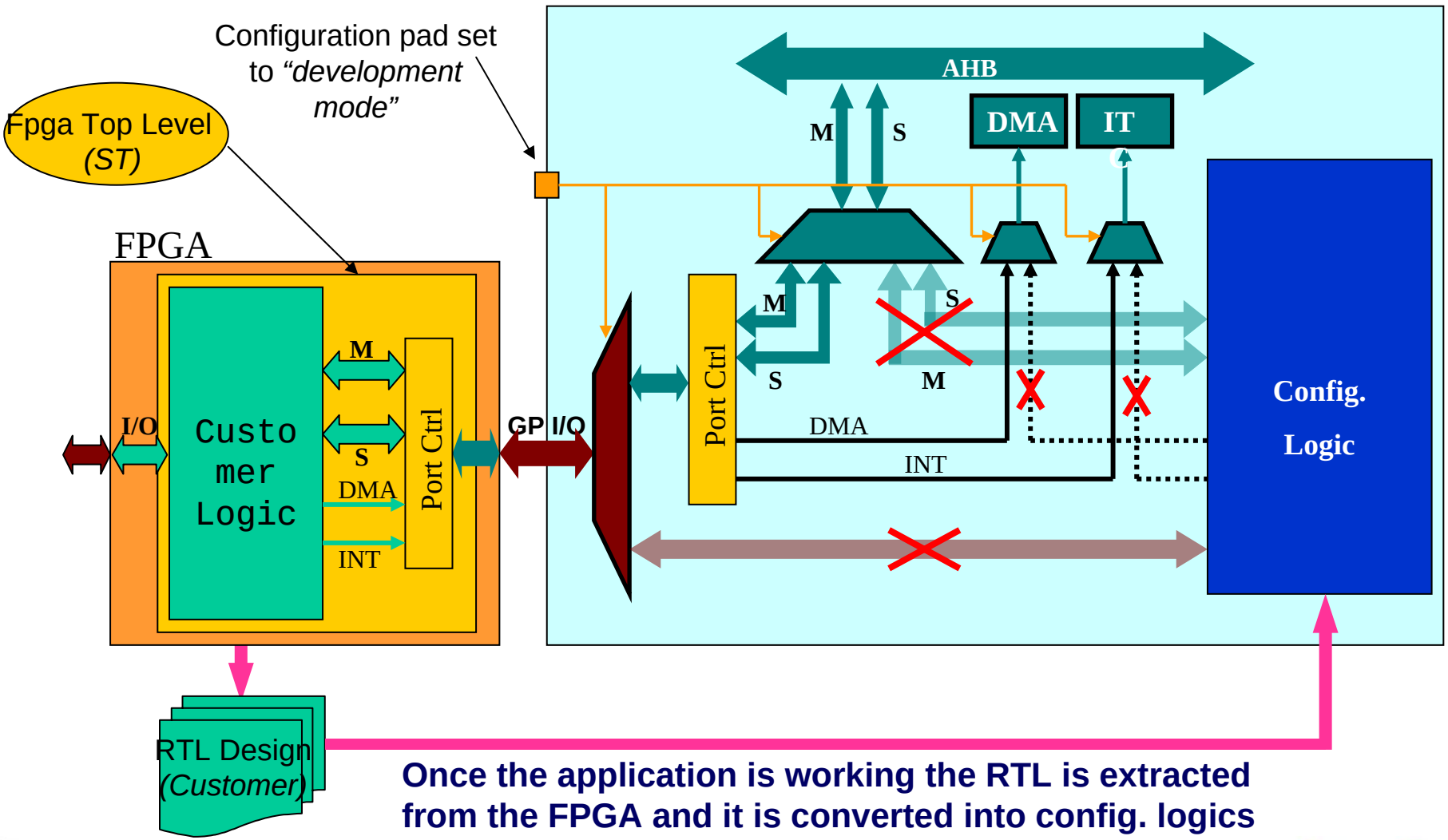
Configurable logic



Support for System Development



Innovative System Development



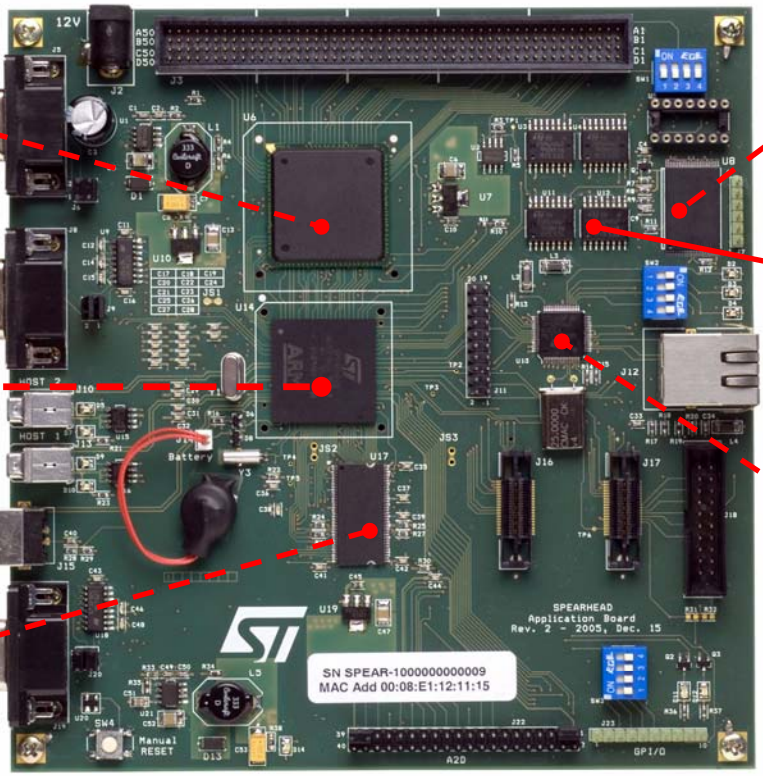
Once the application is working the RTL is extracted from the FPGA and it is converted into config. logics

SPEAr Development Board

FPGA
Xilinx
XC3S4000

SPEARHEAD

32 Mbyte DDR



Flash
For
FPGA

Serial Flashes
Up to 32 MB

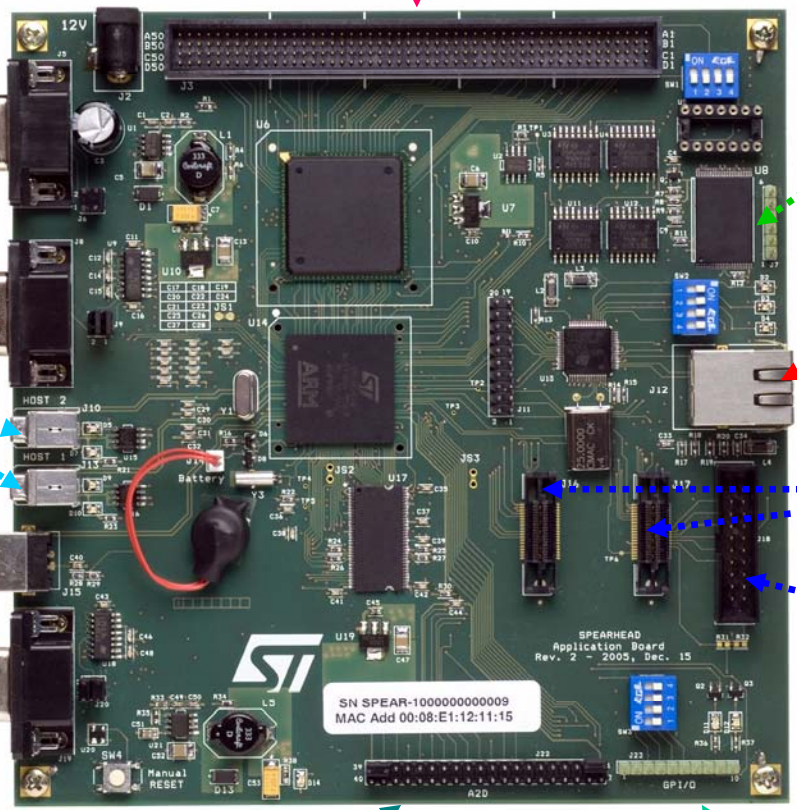
Ethernet PHY

It comes equipped with a suite of drivers for all the peripherals
Supporting Linux and WxWorks Operating Systems
Supporting simple JTAg based emulators

Supporting Multiple Interfaces

Make ASIC easy

Expansion Lines (120 I/Os)



3 Serial I/F

2 USB 2.0 Host Ports HS Capable

1 USB 2.0 Device

FPGA JTAG I/F

Ethernet 10/100

ETM9 I/F 24 bit

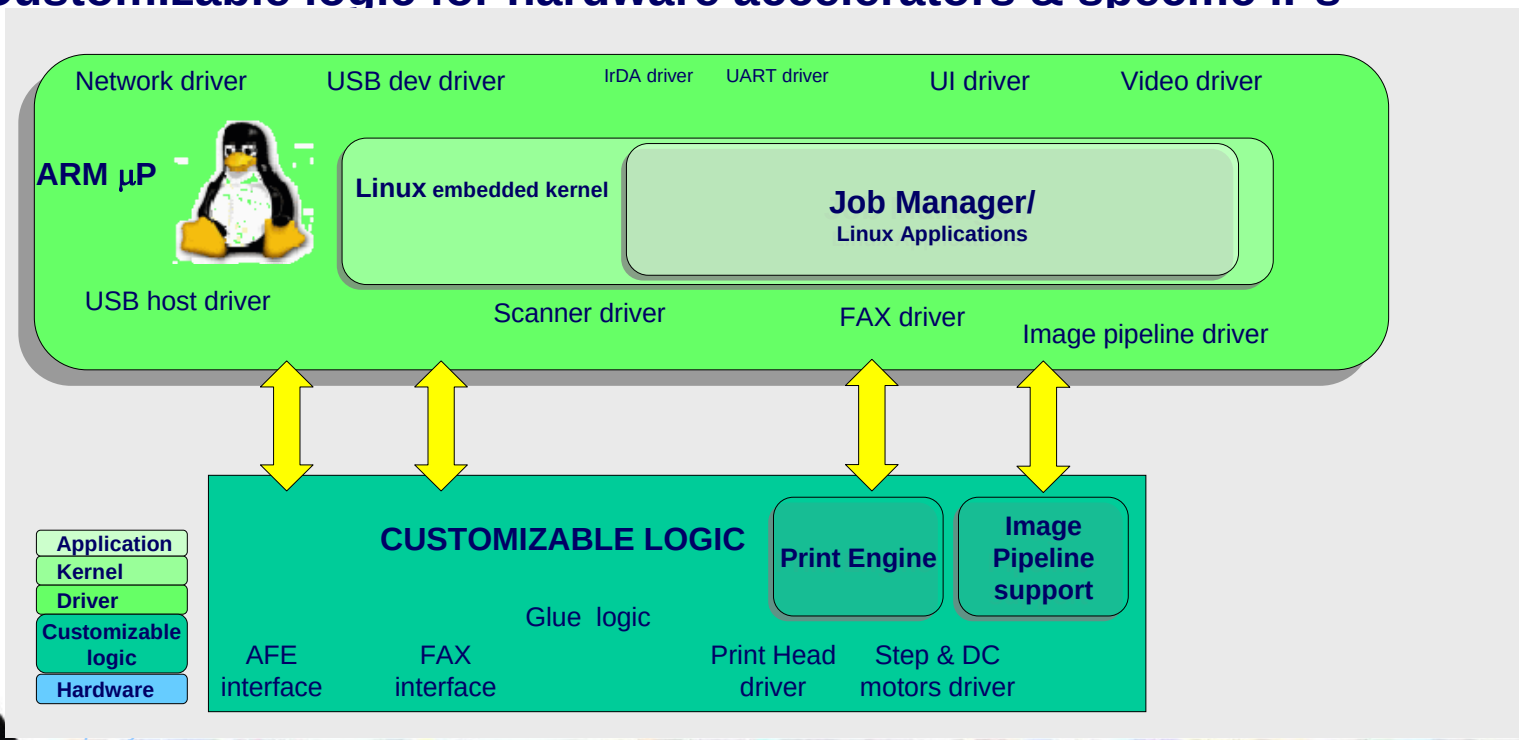
JTAG I/F

16 ADC Channels

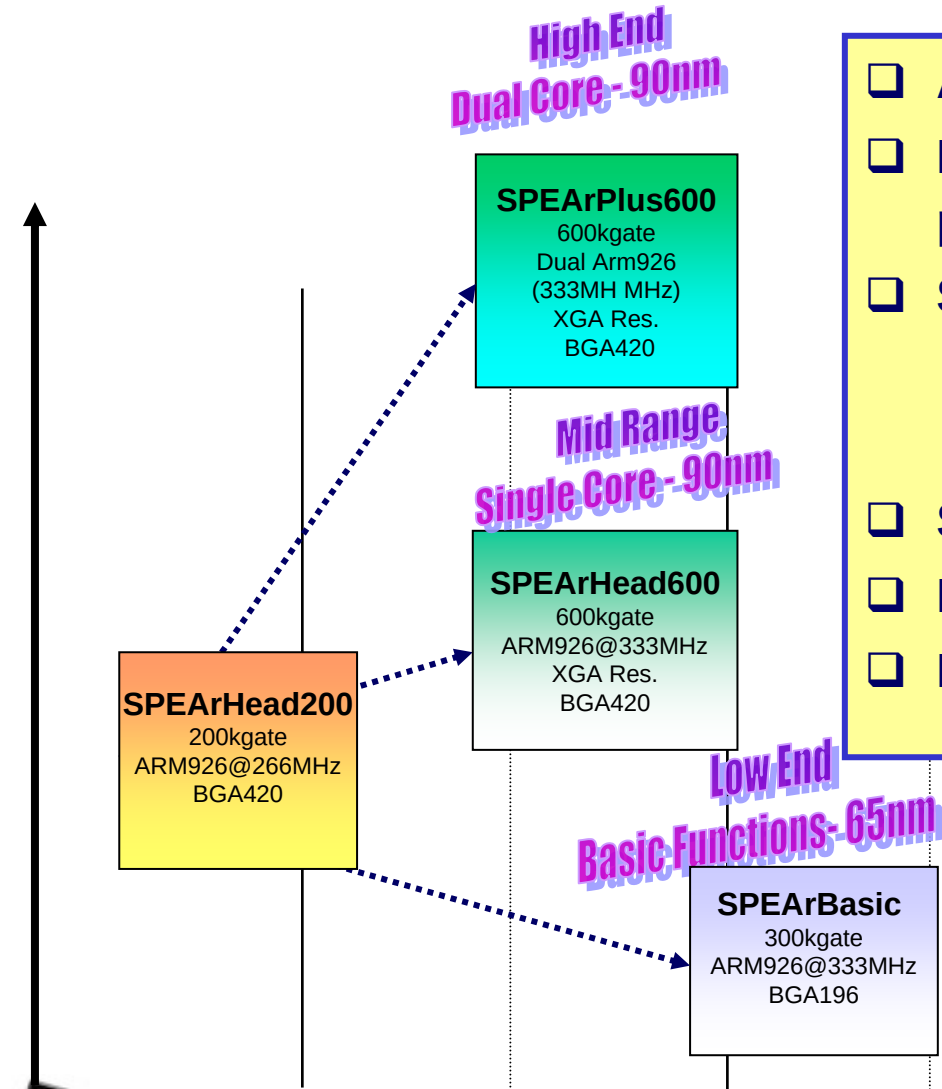
6 GPI/O Lines

FW/SW Partitioning

- ARM core, equipped with Linux (core 2.6.10 Montavista) or VxWorks (extension to Windows CE in evaluation)
  - OS
  - Connectivity
  - Application layers
  - Real time operations
- Customizable logic for hardware accelerators & specific IPs

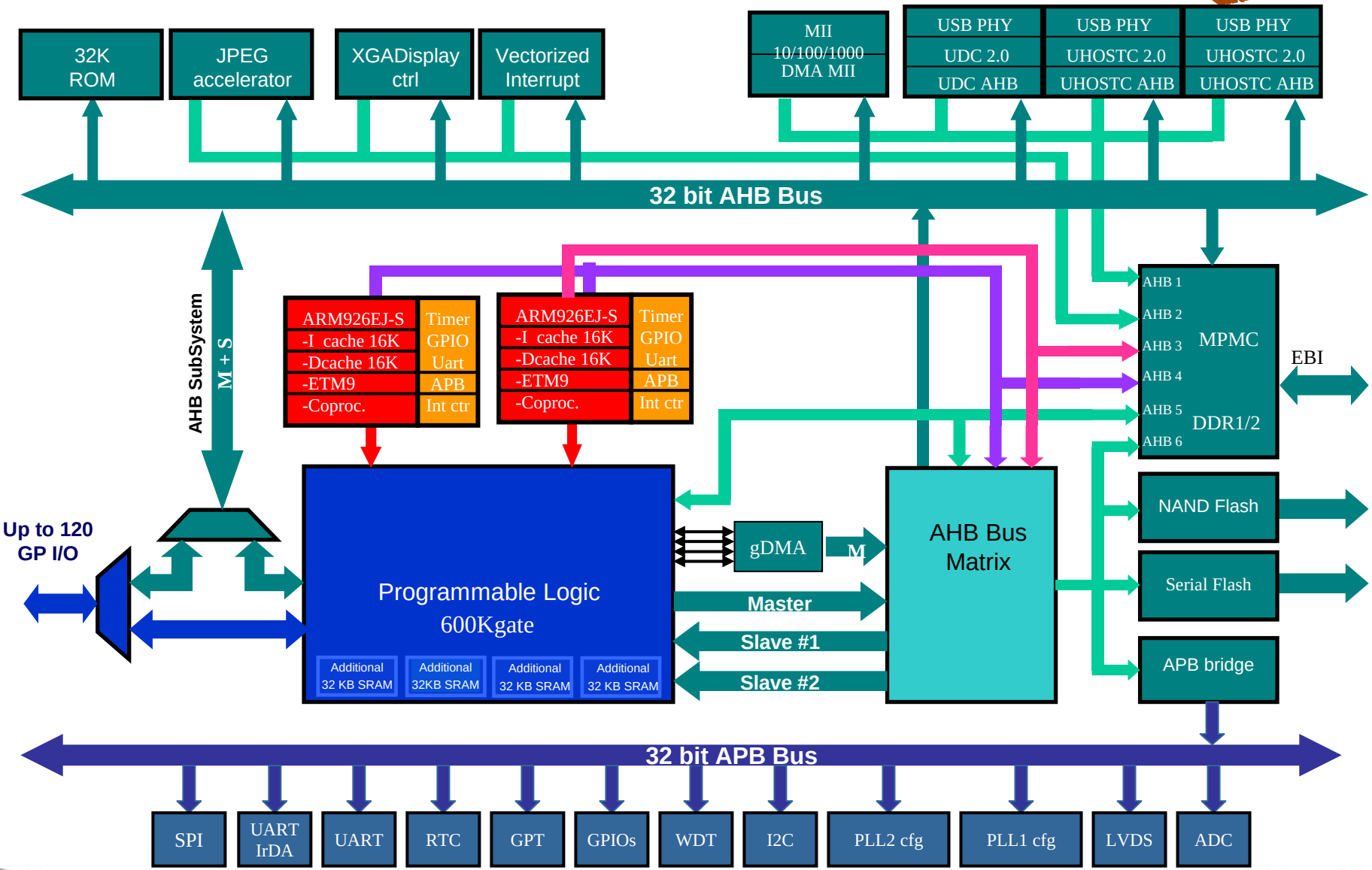


Moving to dual processor: SPEArPlus600



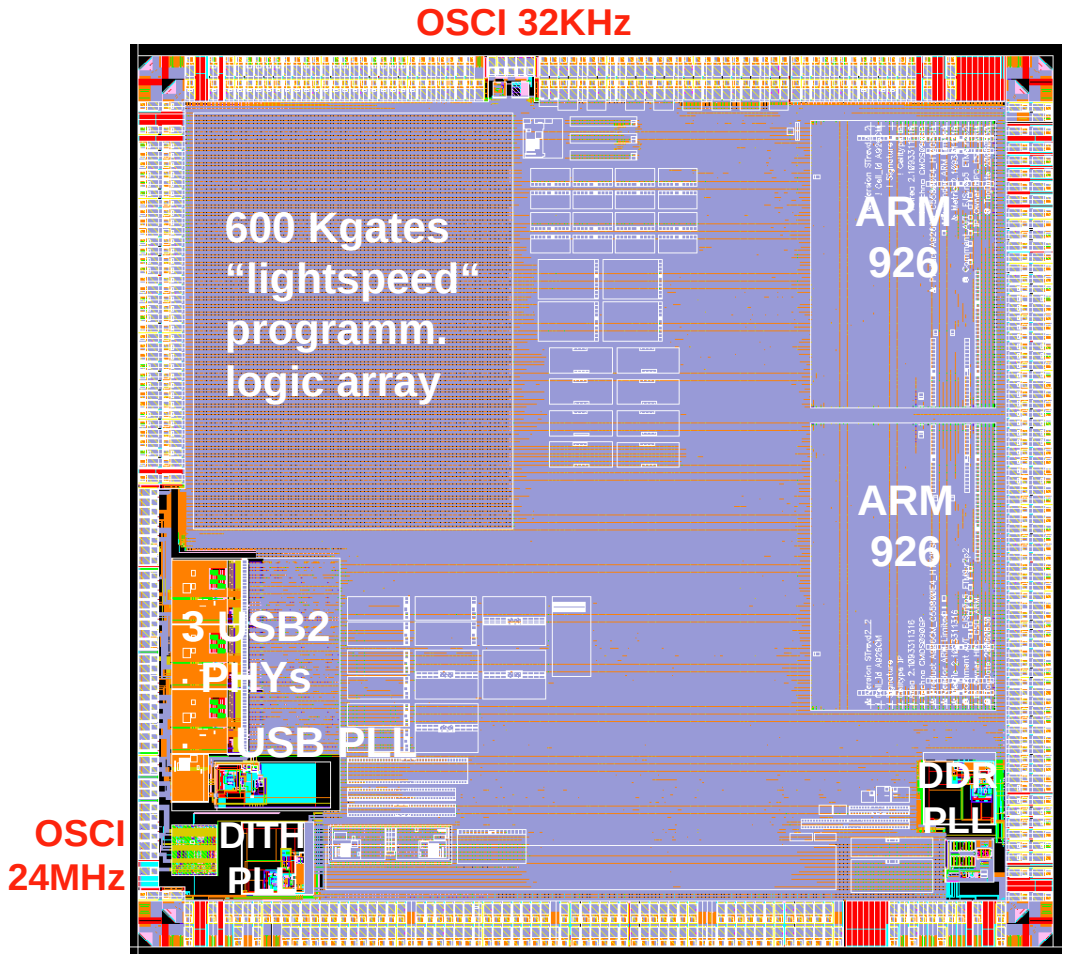
- Addressing market segmentation
- Higher Computation Power with lower power consumption
- Second Arm to boost performance
  - Easier to use than a dedicated DSP
  - Backward compatible
- SPEArPlus silicon in Q1/2007
- Full reference platform for Printers
- Expanding into side applications (NAS)

SPEArPlus600



SPEAr PLUS – 90nm technology

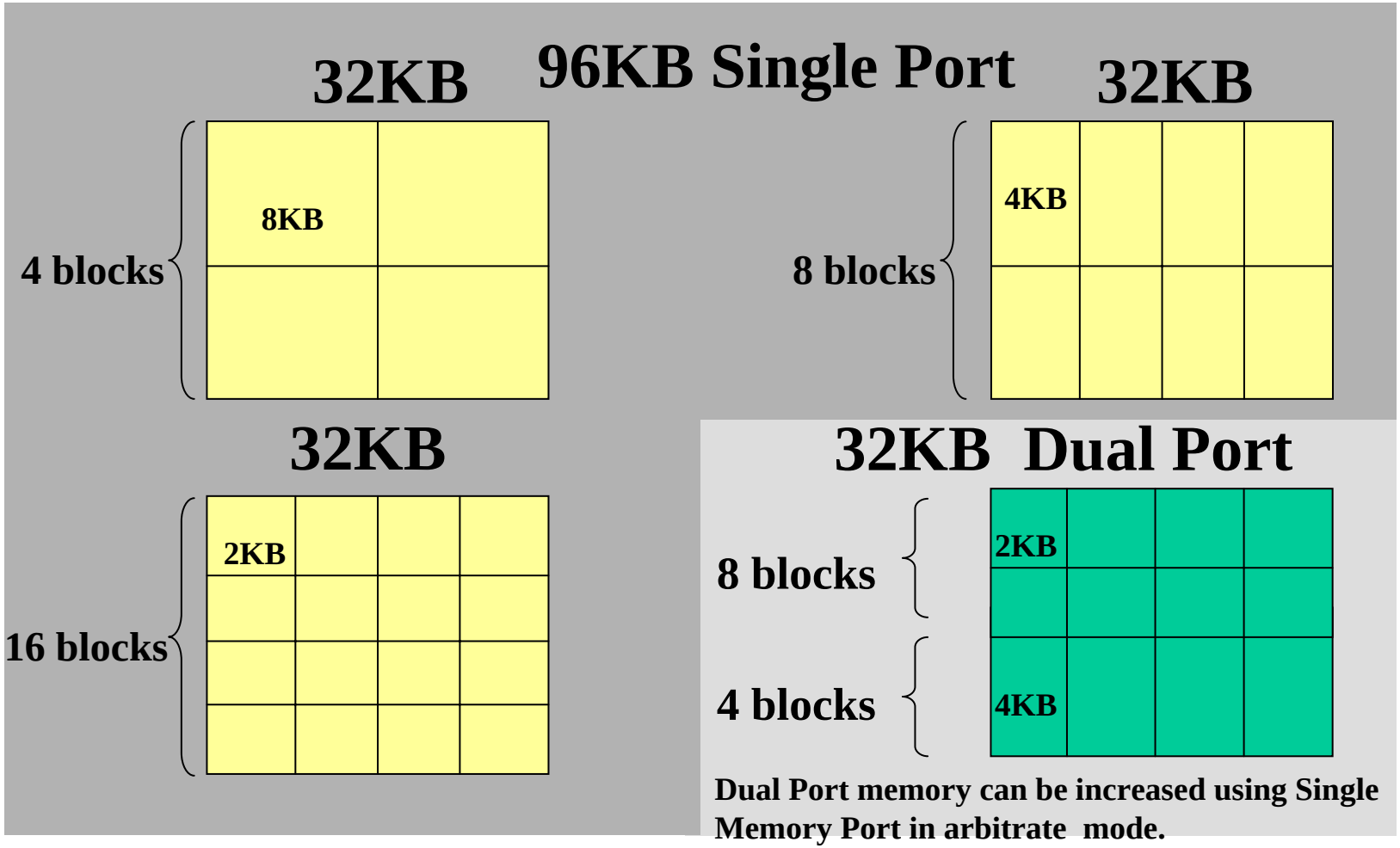
- Main highlights:
  - 600 Kgates progr logic array
  - 2 ARM926EJS @333MHz
  - Dithered Pll
  - 1 USB2.0 device
  - 2 USB2.0 host
  - DDR1+DDR2 COMBO PHY
  - CMOS SRC 3.3V, LVDS 2.5V
  - 2 Oscillators
  - ADC 8 channels, 10bits
- Package: PBGA 420 23x23



Technical Characteristics

- Dual 333Mhz ARM926 16k+16k Architecture
  - Potential TCM extension (up to 32k+32k)
  - 720 (2 x 360) Mips Drystone 2.1
- 600kgate of configurable logic
- From 1 to 4 Metals needed to be specialized
- Ethernet GMAC + USB2.0 Triphy, Timers, RTC, 2 UARTs, 3SPI, IRDA,I^2C
  - USB: 1 Device port + 2 Host ports
- Jpeg accelerator, Display controller XGA 1024x768, color TFT panel
- 4 High Performance Memory controller
  - SDRAM, DDR1/2, Serial Flash, Nand Flash
  - 32bit bus @ 166MHz, total 664 MBytes/Sec
- 136 KB SRAM & 32KB ROM
- High Performance System Architecture
  - High speed I/Os overall throughput: ~ 305MByte/sec
  - Four channel DMA 32bit @ 166Mhz: ~ 664MByte/sec
- Package PBGA 420 balls, 23x23mm, 1 mm pitch

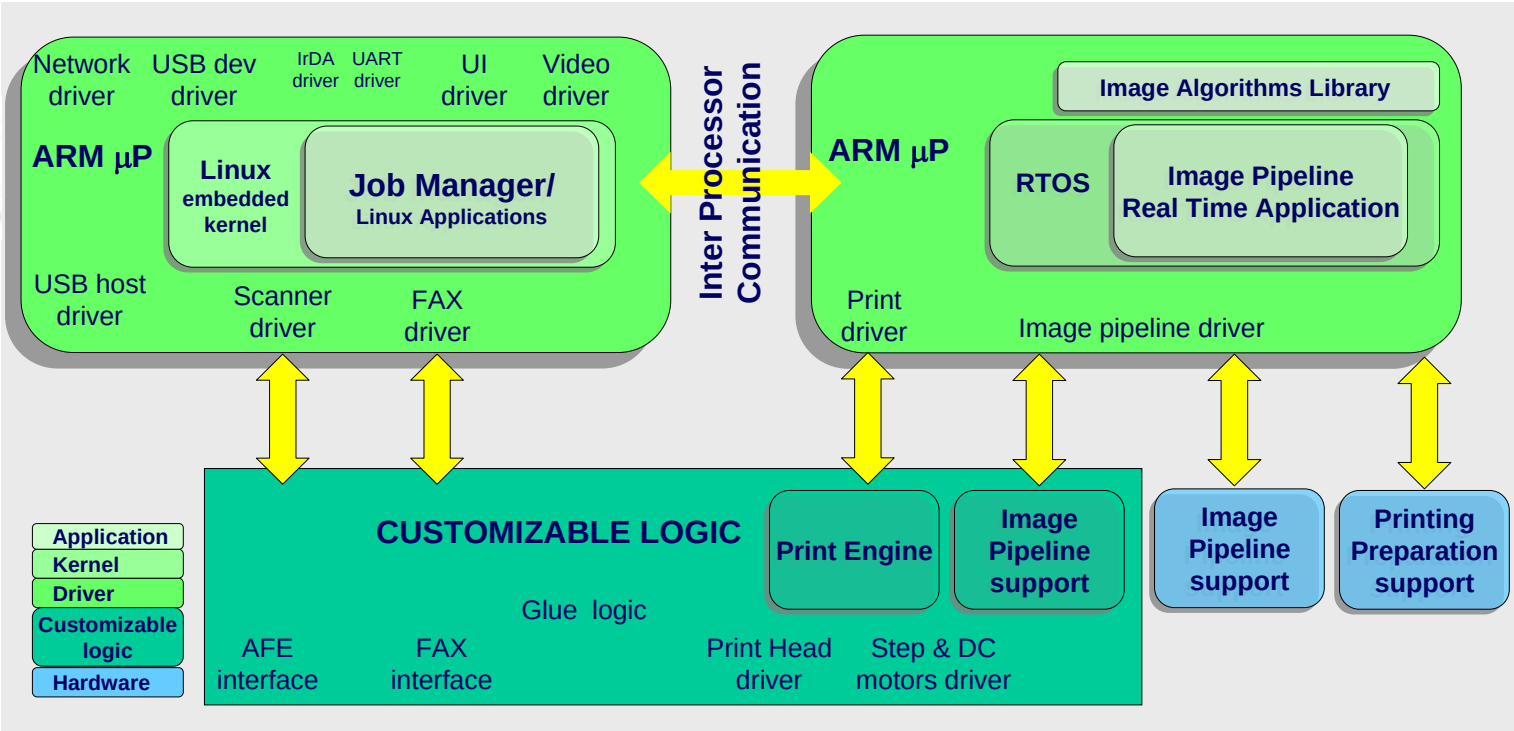
128KB+8KB Internal SRAM memory



Maximum flexibility in grouping memory blocks
• e.g. 10KB= 1 block 8KB+1block 2KB…

Multi – Core FW/SW Partitioning

- ARM 1, equipped with Linux (core 2.6.10 Montavista), is used to run:
  - Job Manager & Connectivity
- ARM2, equipped with RTOS, is used to run:
  - Image pipeline & Real time operations



- Customizable logic for hardware accelerators

Make ASIC easy

Application examples: MPEG4 decoding

Case study: MPEG4 decoder

Full SW solution

- Maximum performances on one ARM926
  - 18fps if ARM running at 266MHz
  - 22fps if ARM running at 333Mhz

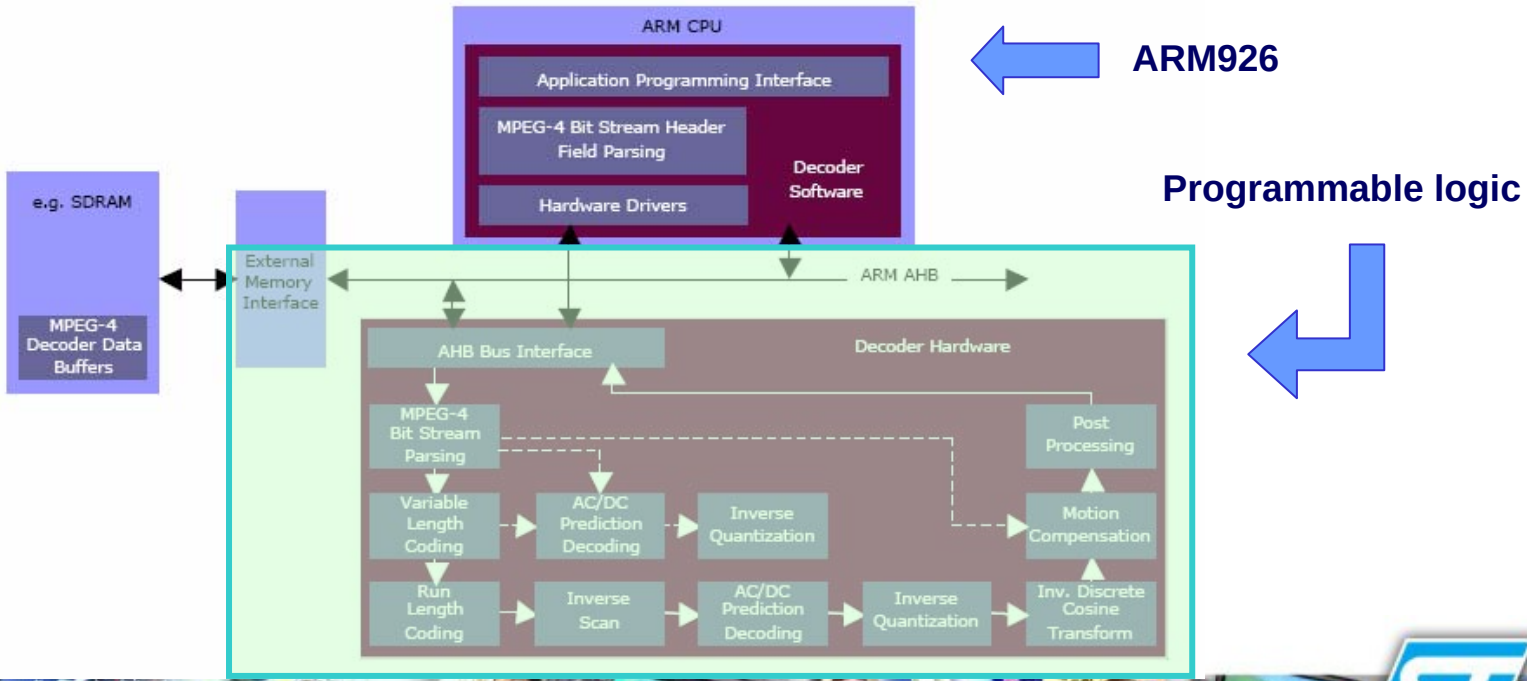
- CPU load for a MPEG4 stream simple profile, lev.0-3

PERFORMANCE REQUIREMENTS				
	QCIF	**QVGA**	**CIF**	**VGA**
Frame Rate	15fps	15fps	30fps	30fps
Bit Rate	64kbps	256kbps	384kbps	1Mbps
External Memory (excl. post processing)	80kB	238kB	313kB	930kB
CPU Load	16MHz	50MHz	130MHz	400MHz
Memory Footprint (inc. program code, ROM data and RAM data)	51kB			

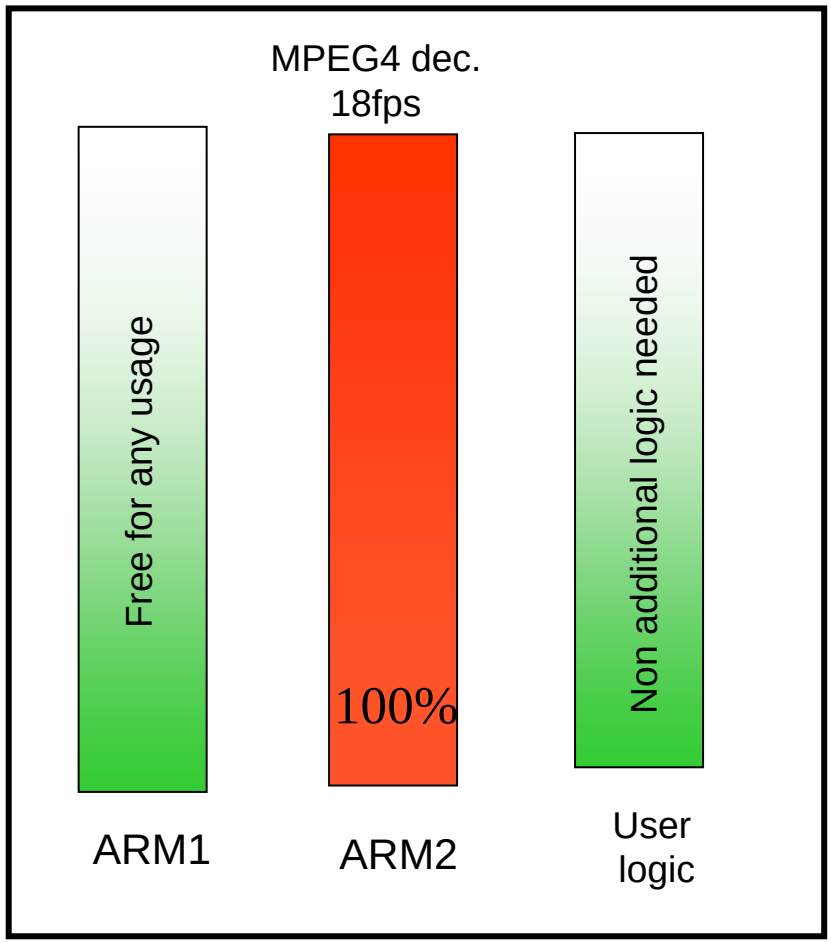
MPEG4 decoder

HW/SW solution

- HW accelerator implemented in programmable logic
  - to accelerate the more complex functions of the SW decoder
  - size of the accelerator is 150kgates + 15kB SRAM running at 66MHz
  - load of CPU is <10MHz
  - VGA resolution 30 fps at 333MHz

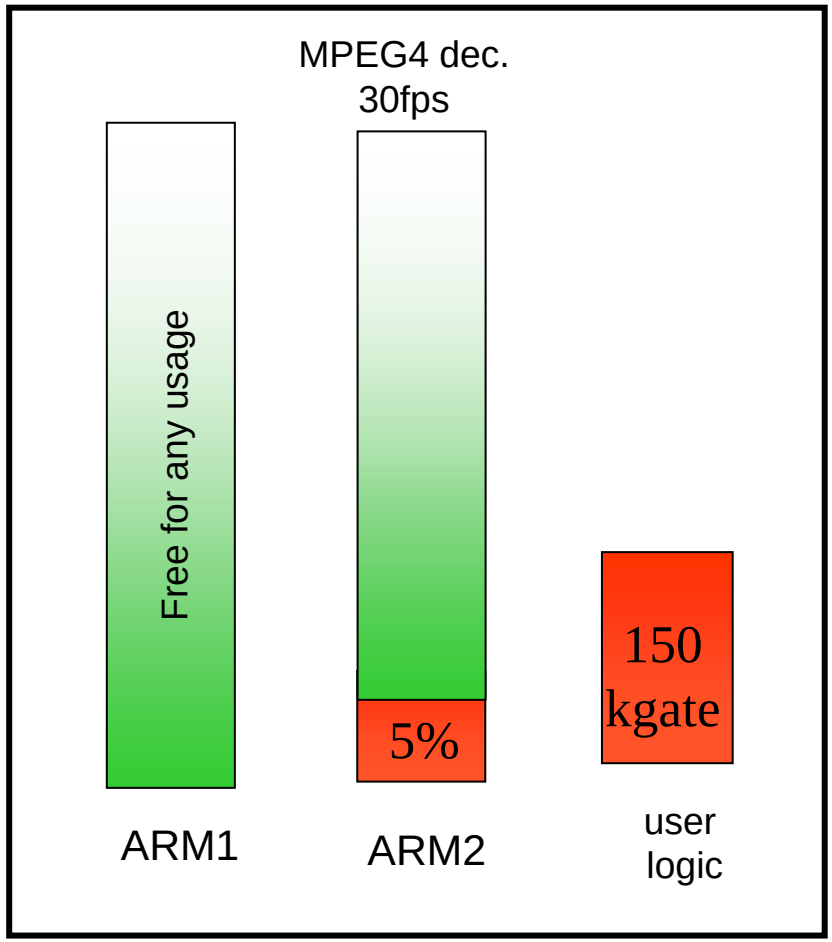


Possible SoC resources usage



Full SW solution

(ARM running at 266Mhz)

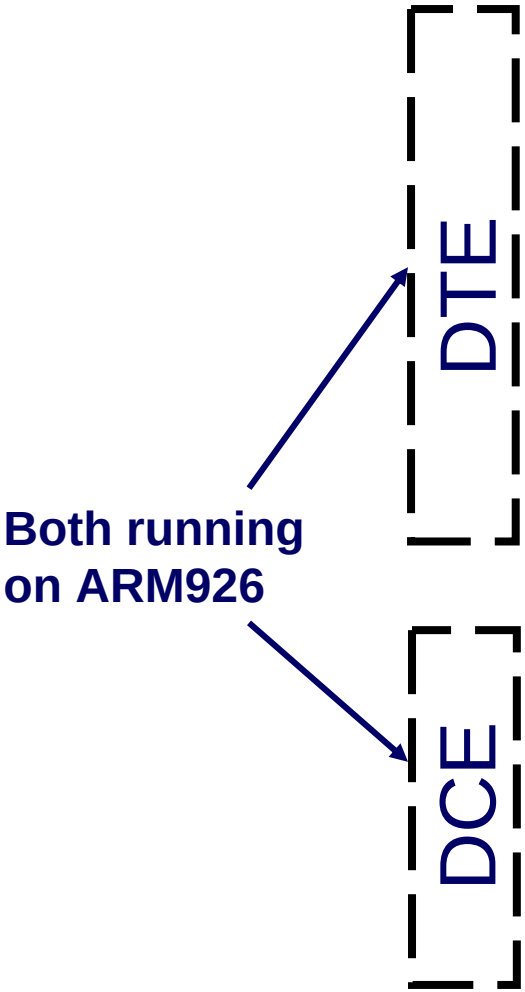


HW/SW solution

Application examples: FAX function

FAX Soft Modem Linux Driver – Class 1

FAX Software – Modem Class 1



FAX APPLICATION

- Image conversion, compression - **ITU-T T.4/T.6**
  - **MH, MR (G3), MMR (G4), JBIG (ITU-T T.82), JPEG (ITU-T T.81)**
- User interface
- Scanning and printing

Manage FAX session (**ITU-T.30**)

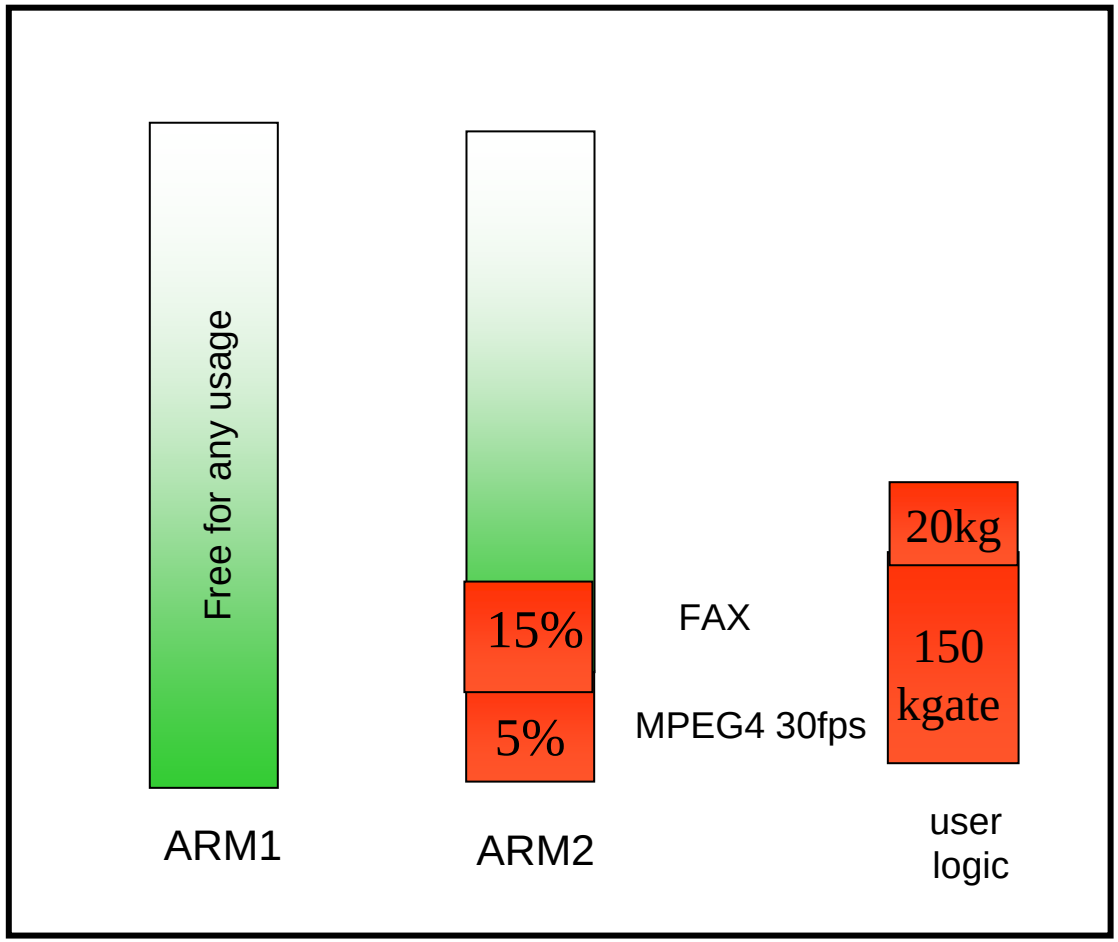
- Exchange and agrees with remote FAX the printing capabilities
- Exchange and agrees with remote FAX the session and transmission capabilities (protocol, speed, ECM, ...)
- Send / Receive data file in blocks / packets
- Implement retransmission of bad packets (ECM option)

Interface between Application and Driver with AT CMD (**Class 1**) – ITU-T T.31

FAX (Soft) Modem DRIVER - (**Class 1**)

- Linux serial driver interface
- AT CMD interpreter (**ITU-T T.31**)
- Modem state machine
- Connection protocol **(ITU-T V.21)** with remote FAX
- Data Modulation (**DATA PUMP**) – **V27ter, V.29, V.17, V.34 H/D**
- Interface with HW driver **(STLC7550)**

Possible SoC resources usage

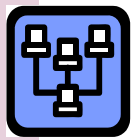


(ARM running at 266Mhz)

Conclusions

- SpearPlus architecture opens the door to unprecedented flexibility
  - HW configurability
  - dual core SW configurability
- Symmetrical dual core architecture for maximum flexibility
  - Possibility to map different OS
  - Possibility to access all the peripherals from the 2 cores
  - Possibility to access programmable logic from the 2 cores
- HW flexibility
  - configurable logic on board
  - possibility to use embedded SRAm as TCM of ARM cores

Moving to dual processor



Standard IPs & Special IOs:
connectivity and interactions

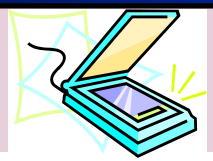
Support for System Development

ARM926EJ
-I cache 16
-Dcache 16
-ETM9
-Coproc.
Timer
GPIO
Uart
APB
Int cu

ARM926EJ
-I cache 16
-Dcache 16
-ETM9
-Coproc.
Timer
GPIO
Uart
APB
Int cu

State of Art Architecture

Programmable Logic



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